UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/602,596	06/25/2003	Wataru Saito	239400US2S	1453

22850 7590 04/21/2005

OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
OWENS, DOUGLAS W	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 04/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/602,596	SAITO ET AL.	
	Examiner	Art Unit	
	Douglas W. Owens	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *22,26 and 27* is/are allowed.

6)☒ Claim(s) *1-4,6,7,9-15,21 and 25* is/are rejected.

7)☒ Claim(s) *8,16-20,23-25 and 28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1 – 4, 6, 7, 9 – 15 and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,693,338 to Saitoh et al.

Regarding claims 1 and 21, Saitoh et al. teach a power semiconductor device (Fig. 6, for example), comprising:

a first semiconductor layer (11) of the first conductivity type;

a second semiconductor layer (19) of the first conductivity type and two third semiconductor layers (18) of a second conductivity type which are alternately and laterally arranged on the first semiconductor layer;

a first main electrode (16) in electrical contact with the first semiconductor layer;

a fourth semiconductor layer (12) of the second conductivity type selectively formed in surface regions of the second and third semiconductor layers;

a fifth semiconductor layer (13) of the first conductivity type selectively formed in a surface region of the fourth semiconductor layer;

wherein the first to fifth semiconductor layers are constituted by a silicon layer (Col. 46, lines 17 – 20);

a second main electrode (17) formed in contact with surfaces of the fourth and fifth semiconductor layers; and

a control electrode (15) formed on surfaces of the second, fourth and fifth semiconductor layers,

wherein an insulating material (22) is interposed between the second and third semiconductor layers;

wherein an impurity concentration of the first semiconductor layer is lower than that of the second semiconductor layer (Col. 8, lines 9 – 20; Col. 10, lines 26 – 30) and a layer thickness ratio A is given by an expression:

$0 + A = t/(t+d) \# 0.72$ (Col. 8, lines 5 – 7)

where t is a thickness of the first semiconductor layer, and d is a thickness of the second semiconductor layer; and

wherein assuming that a breakdown voltage is represented by VB, then VB, t, B and A satisfy the relationship,

$t < 2.53 \times 10^{-6} \times (A \times VB)^{7/6}$ (cm), since the device disclosed by Saitoh et al. is identical to that of the instant application. For example, t (first semiconductor layer, 11) can be selected to be 15 microns, and d (second semiconductor layer, 19) can be 7 microns, which would result in a ratio of 0.68. The ratio would be within the desired ratio discussed in lines 2 – 7 of column 8, and shown graphically in Fig. 3A. The range of thicknesses that would result in a functioning device, while maintaining the desired

range, is considered to be disclosed inherently by Saitoh et al., just as it is considered to be disclosed in the instant application, which does not explicitly disclose all possible combinations of thicknesses. The proposed values would result in the expression, 2.53 x 10^{-6} x $(A \times VB)^{7/6}$ (cm) being equal to about 28.2, which is greater than the thickness t, of 15 microns.

Regarding claim 2, Saitoh et al. teach a semiconductor device, wherein, assuming an aspect ration B is represented by B = d/w (d = 7 microns, for example), where w is an interval between adjacent third semiconductor layers (w = 8 microns, for example; Col 8, lines 20 – 21), the layer thickness ratio A (A = 0.68, for example; discussed above) and the aspect ratio B (B = 0.87) satisfy an expression below:

A x B # 1.15,

since A x B = 0.596.

Regarding claim 3, Saitoh et al. teach a semiconductor device, wherein an aspect ration B and the layer thickness ration A satisfy an expression below:

-0.04B + 0.48 < (A x B) < 0.13B + 0.59.

since 0.445 (left term) is less than 0.596 (middle term), which is less than 0.704 (right term).

Regarding claim 4, Saitoh et al. teach a device, wherein A x B satisfies the relationship:

0.58 < (A x B) < 0.71,where A = 0.68, for example.

Regarding claim 6, Saitoh et al. inherently teach a device, wherein Nn, VB and A satisfy the relationship,

$Nn > 1.11 \times 10^{18} \times (A \times VB)^{-4/3}$ (cm^{-3}), since the device disclosed by Saitoh et al. is identical to that of the instant application. Moreover, Saitoh et al. teach the optimal impurity concentration of the first semiconductor layer, as disclosed on page 17 of the instant application, in lines 10 and 11 of column 8.

Regarding claim 7, Saitoh et al. teach a device (Fig. 6), wherein an insulating material (22) is interposed between the second and third semiconductor layers.

Regarding claims 9 – 15, Saitoh et al. teach a device, wherein an impurity concentration profile at least one of the second semiconductor layer and third semiconductor layer reduces with depth. This feature is shown in Fig. 4c, where the impurity concentration gradually reduces near the junction with the first semiconductor.

Allowable Subject Matter

3. Claims 8, 16 – 20, 23-25 and 28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. Claims 22, 26 and 27 are allowed.

Response to Arguments

5. Applicant's arguments filed March 30, 2005 have been fully considered but they are not persuasive.

Applicant argues that Saitoh et al. do not teach an embodiment that satisfies the expressions, $0 + A = t/(t+d)\#0.72$ and $t < 2.53 \times 10^{-6} \times (A \times VB)^{7/6}$ (cm). The crux of the disclosure of Saitoh et al. is to form a device, wherein the ratio of the first layer to the sum of the first and second layer remains within a specific range (See, Fig. 3A for

example) for the purpose of reducing on resistance. For example, t (first semiconductor layer, 11) can be selected to be 15 microns, and d (second semiconductor layer, 19) can be 7 microns, which would result in a ratio of 0.68. The ratio would be within the desired ratio discussed in lines 2 – 7 of column 8, and shown graphically in Fig. 3A. The range of thicknesses that would result in a functioning device, while maintaining the desired range, is considered to be disclosed inherently by Saitoh et al., just as it is considered to be disclosed in the instant application, which does not explicitly disclose all possible combinations of thicknesses. The instant application only cites specific thicknesses of t=14.1, and the ratio B being equal to 2, which would require d to be 16. In the cited example, the expression $-0.04B + 0.48 < (A \times B) < 0.13B + 0.59$ **is not satisfied, since the right side of the inequality is 0.85**, which is less that A x B (0.94). **It is of note that the instant application does not recite one single example wherein the expression of claim 1 is satisfied**. However, the application is interpreted from the viewpoint of one having ordinary skill in the art. Accordingly, the disclosure is enabling and the appropriate thicknesses are considered to be disclosed. This also applies in the disclosure of Saitoh et al. However, Applicant is welcome to submit proposed values that would satisfy the expression of claim 1. The proposed values would result in the expression, $2.53 \times 10^{-6} \times (A \times VB)^{7/6}$ (cm) being equal to about 28.2, which is greater than the thickness t, of 15 microns.

Moreover, the disclosure of Saitoh et al. is sufficient for one having ordinary skill in the art to arrive at specific values of t and d (the thickness of the first and second drift layers) to arrive at the ratio disclosed by Saitoh et al. in lines 5 – 8 of column 8. For

example, the value for t selected in the example provided in the rejection was 15. However, many other values could be used to satisfy the ratio provided by Saitoh and the expression of the instant application. In one example Saitoh discloses using 26 microns for t. The first drift layer, t could also be formed to be 25.5 microns thick, with the second drift layer, d being 11.9 microns thick. In this example, which is much closer to one of the specific examples cited, the expression equals 28.2, which is still less that t, 25.5. Further yet, t can be selected to be 26 microns, with d at 12.133, the ratio disclosed by Saitoh et al. is satisfied, since 0.682 lies between 0.21 and 0.8. These values also satisfy the expression of the instant application with t being 26 microns, which is less than 28.2, the value of the right side of the inequality.

Applicant further asserts that the proposed values presented as examples in the rejection above would have resulted in a 400 Volt device instead of a 600 Volt device. This is a mere assertion with no supporting evidence. However, assuming that this assertion is correct, the expression would still be satisfied with the values suggested above since t, having a value of 15 microns is less than the right side of the inequality, which would be 17.6 microns for a 400 Volt device.

Applicant has selected another example, where t is equal to 13 microns and d is 30 microns to argue that the disclosure of Saitoh et al. does not satisfy the expression of claim 1. Note that when t is equal to 13 microns, d can also be about 6 microns to meet a desired ratio of 0.68, which lies between 0.21 and 0.8. This would also result in a value of 28.3 on the right side of the expression, which is greater than t.

Applicant argues that Saitoh et al. do not disclose an insulating film interposed between the second and third semiconductor layers. This teaching can be seen in Figure 6.

Allowable Subject Matter

6. Claims 22, 26 and 27 are allowed.

7. Claims 8, 16 – 20, 23 – 25 and 28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas W. Owens whose telephone number is 571-272-1662. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Douglas W Owens
Examiner
Art Unit 2811

DWO